大实验答辩

GROUP 24

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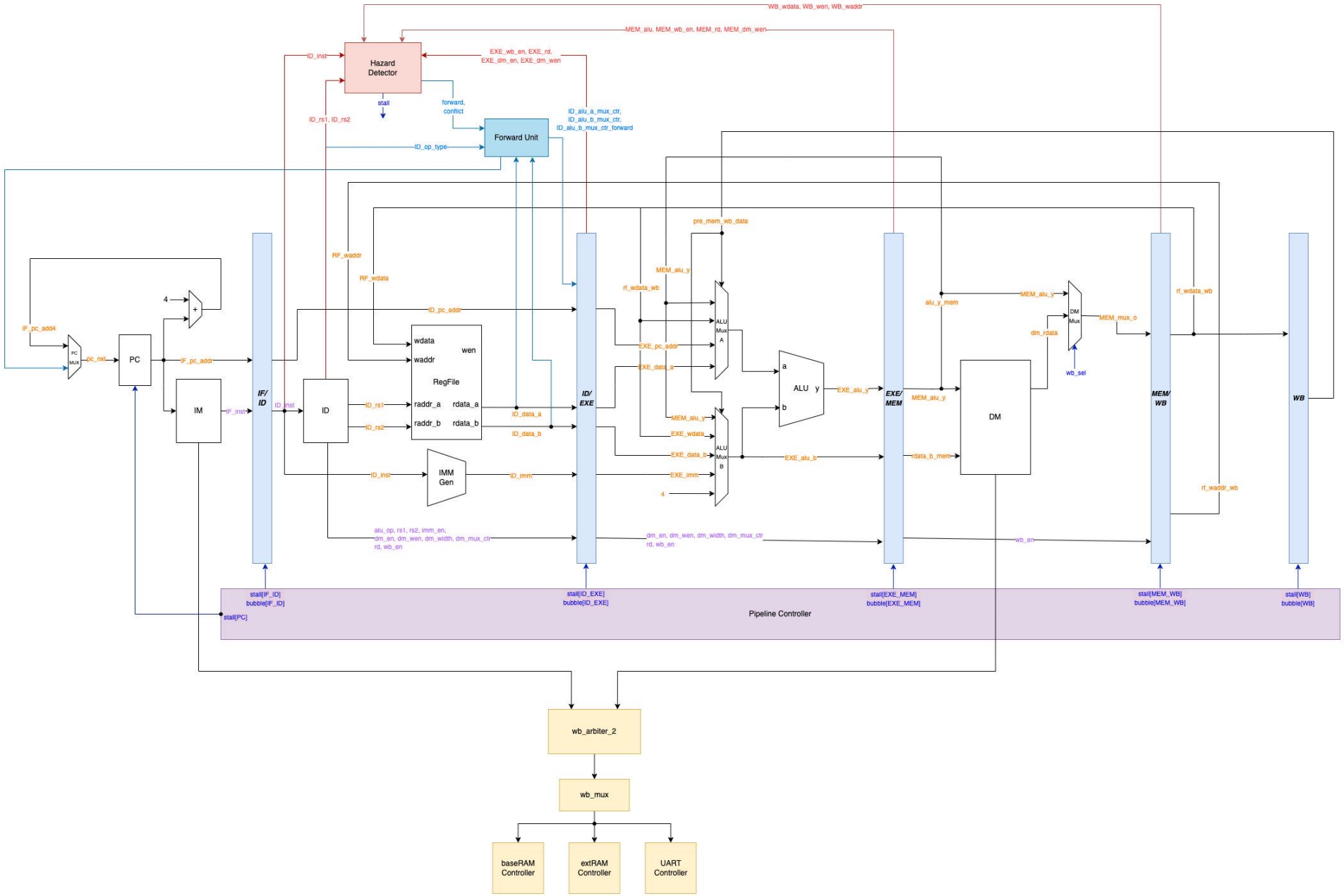
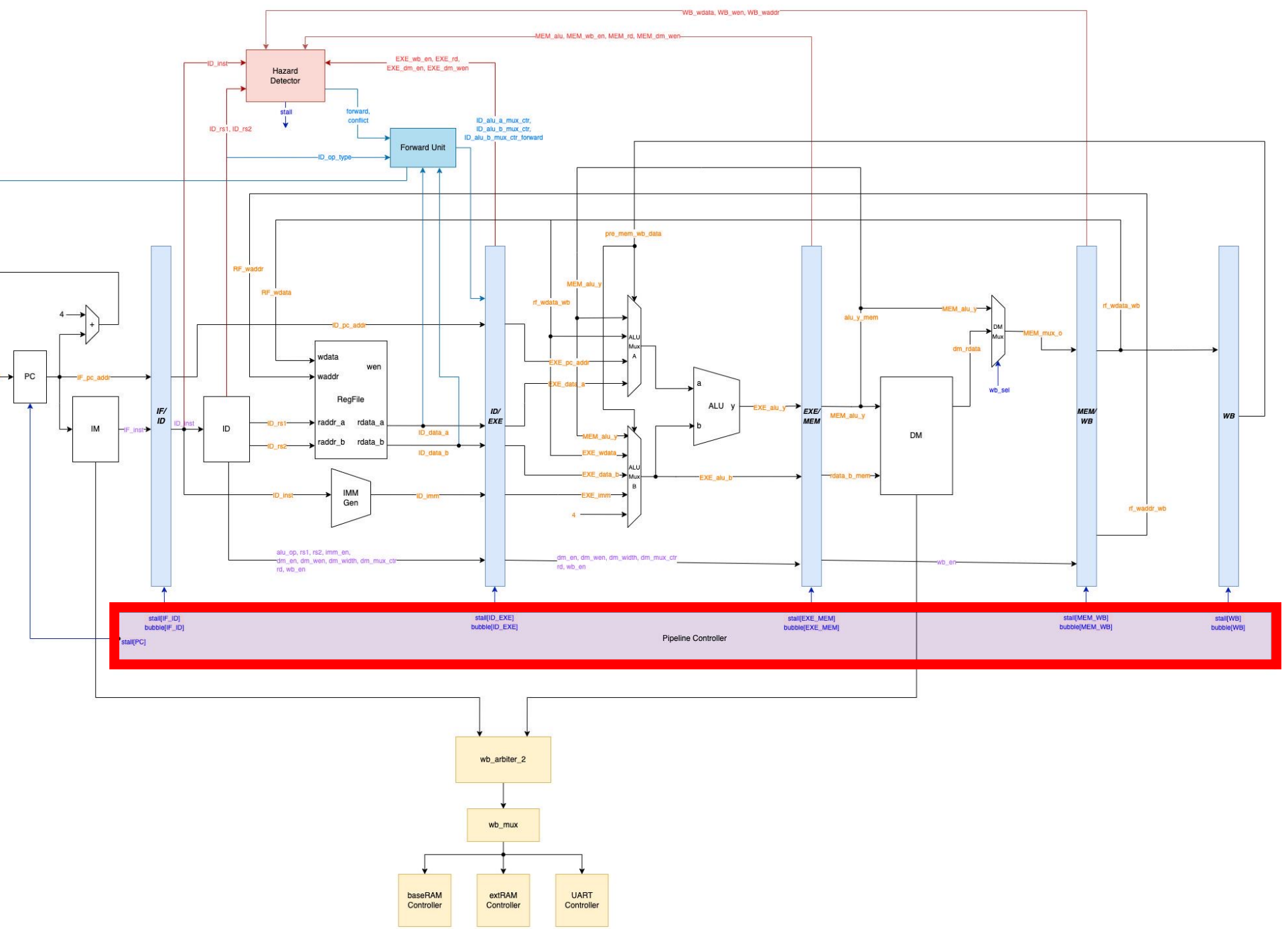
整体设计 & 数据通路

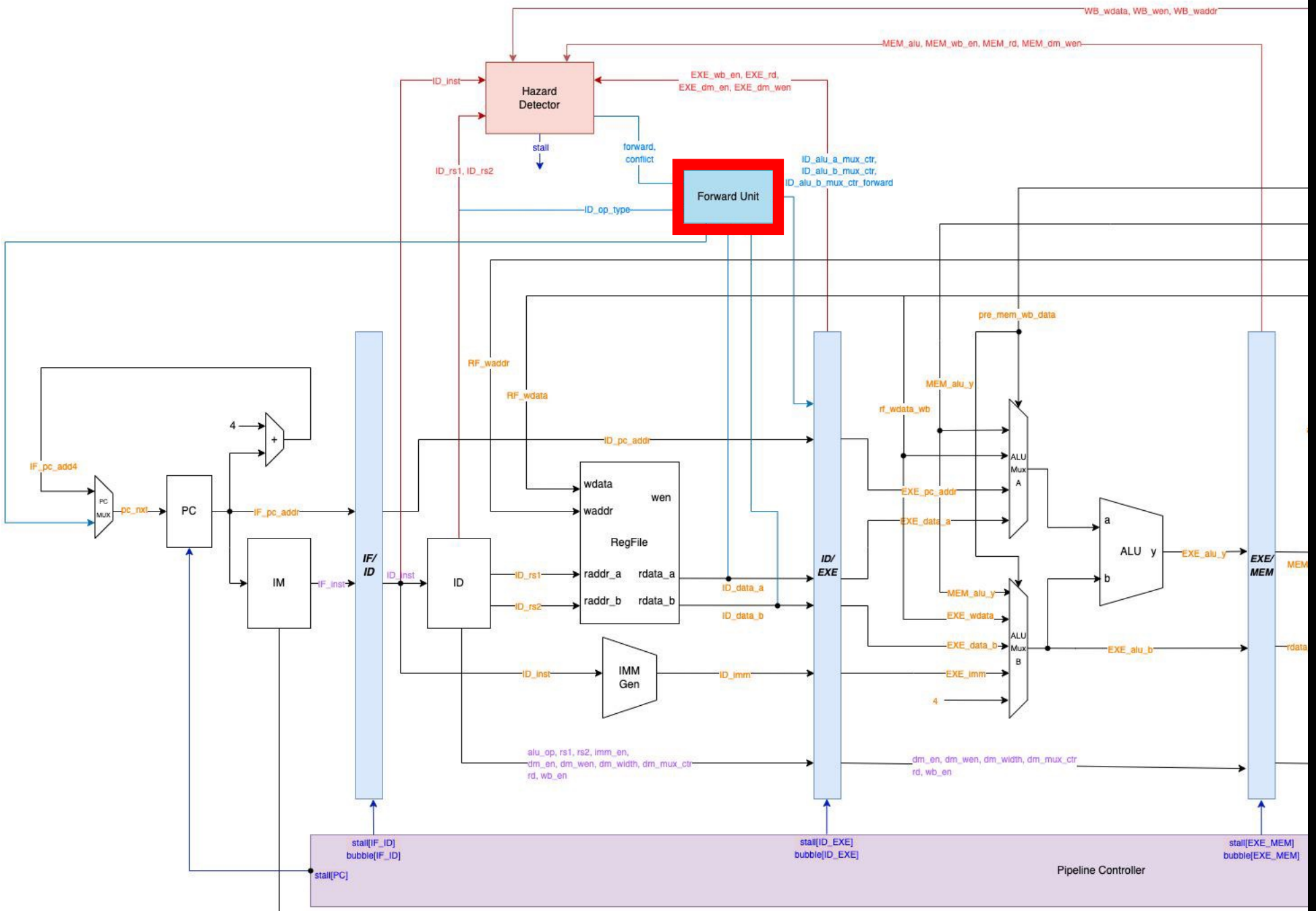


- 五级流水线
- Wishbone总线
- 控制器
- 数据旁路
- 冲突检测



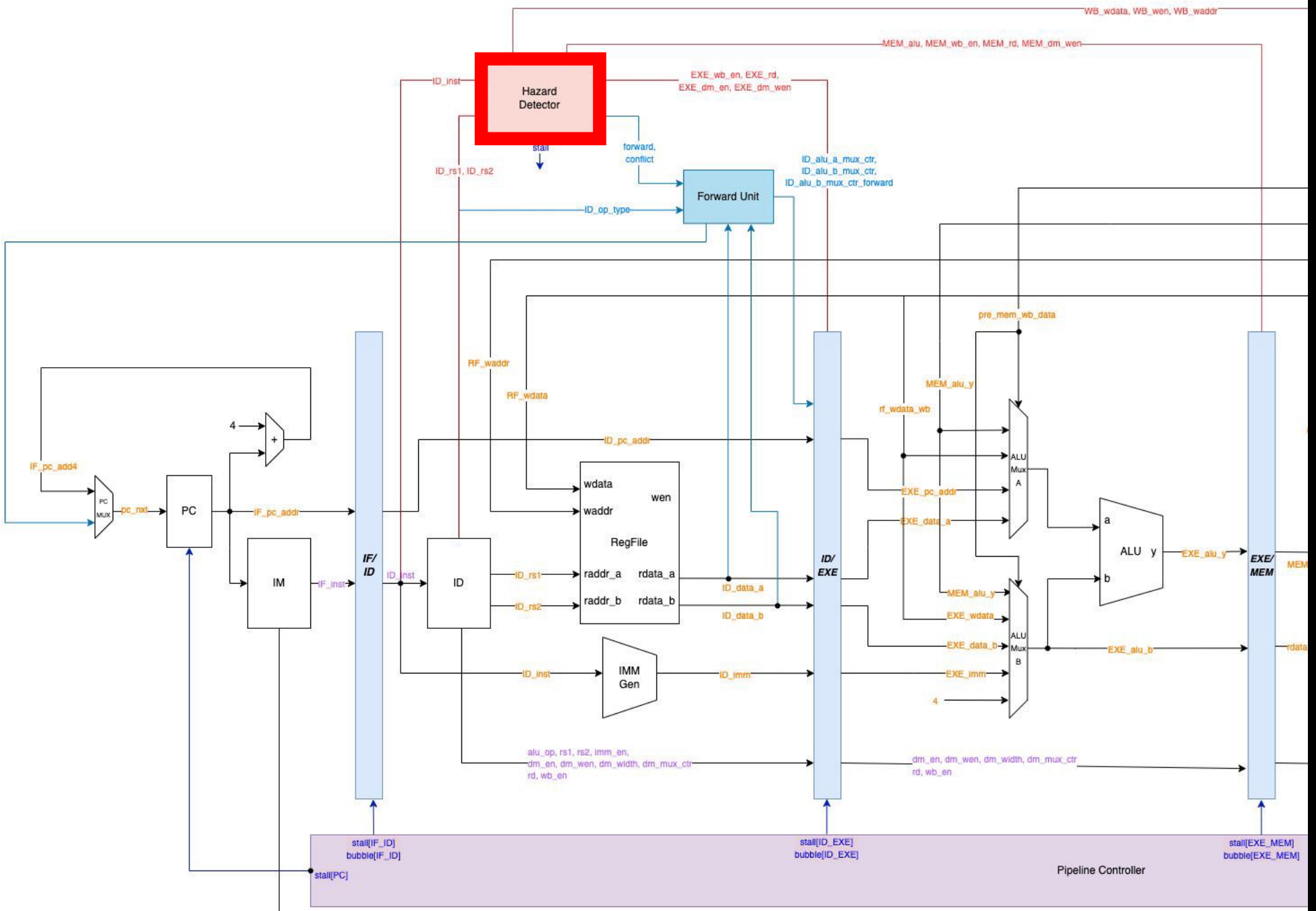
控制器

- 6位宽度向量
- DM/IM内存读取
- 冲突控制
- 跳转指令



数据旁路

- 跳转地址处理
- 根据冲突检测信号进行数据前传



冲突检测

- 控制冲突
- 数据冲突

中断异常

➢实现指令：

- ecall、ebreak、mret
- csrrw、csrrs、csrrc

➢异常处理&读写csr寄存器

- 集成一个模块，在 MEM 段
- 处理 load 类数据冲突

➢时钟中断：

- csr_mtimer 模块
- 管理 mtime 和 mtimecmp
- 实现单独的wishbone slave

效果展示

性能测试主频80MHZ

```
C:\Users\moon\Desktop\source_
1
connecting to 166.111.226.111
MONITOR for RISC-V - initiali
running in 32bit, xlen = 4
>> g
addr: 0x800010a8

elapsed time: 1.809s
>> g
addr: 0x80001008

elapsed time: 35.233s
>> g
addr: 0x80001024

elapsed time: 19.086s
>> g
addr: 0x80001080

elapsed time: 33.976s
```

```
C:\Users\moon\Desktop\source_
1
connecting to 166.111.226.111
MONITOR for RISC-V - initiali
```

中断异常和ECALL

```
>> a
addr: 0x80400000
one instruction per line, empty line to end.
[0x80400000] li t0, 1
[0x80400004] li t1, 0
[0x80400008] loop:
[0x80400008]     addi t0, t0, 1
[0x8040000c]     bne t0, t1, loop
[0x80400010] jr ra
[0x80400014]
>> g
addr: 0x80400000
killed timeout program.

elapsed time: 0.125s
>> a
addr: 0x80410000
one instruction per line, empty line to end.
[0x80410000] li s0, 30
[0x80410004] li a0, 84
[0x80410008] ecall
[0x8041000c] li a0, 72
[0x80410010] ecall
[0x80410014] li a0, 85
[0x80410018] ecall
[0x8041001c] li a0, 67
[0x80410020] ecall
[0x80410024] li a0, 83
[0x80410028] ecall
[0x8041002c] li a0, 84
```

EBREAK

```
[0x80420010] li t3,4
[0x80420014] jr ra
[0x80420018]
>> g
addr: 0x80420000

elapsed time: 0.000s
>> r
R1 (ra)     = 0x8000034c
R2 (sp)     = 0x807f0000
R3 (gp)     = 0x00000000
R4 (tp)     = 0x00000000
R5 (t0)     = 0x00000001
R6 (t1)     = 0x00000002
R7 (t2)     = 0x00000000
```

谢谢！